12 770101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

priority Application Serial No. 08/582,385
priority Filing Date ..... January 3, 1996
Inventor ..... G. Sandhu
Assignee ..... Micron Technology, Inc.
priority Group Art Unit 2109
Examiner ..... unknown
Attorney's Docket No. MI22-713
Title: Capacitor Constructions (As amended)

PTO TRANSMITTAL LETTER
(Divisional Application Under Rule 1.60(b))

To: Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Wells, St. John, Roberts
Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99204-0317
Telephone: (509) 624-4276
Fax: (509) 838-3424

Enclosed are:

1. Return Postcard Receipt;
2. A check in the amount of $770;
3. PTO Transmittal letter;
4. Request for Divisional Application under Rule 1.60(b) (incl. copy of parent application comprising Title page, plus 28 total pages specification, claims and abstract; drawings (Figs. 1-22) and declaration).
5. 12 sheets of formal drawings.
6. Preliminary Amendment.
7. Information Disclosure Statement including PTO-1449.

The Commissioner is hereby authorized to charge payment of fees or credit overpayments to Deposit Account No. 23-0925 in connection with: any patent application processing fees under 37 CFR 1.17; and any additional filing fees under 37 CFR 1.16 for the presentation of extra claims.

Respectfully submitted,

Date: 7/1/97

By: _____
Title:Attorney/Agent for Applicant
David G. Latwesen, Ph.D.
Reg. No.: 38,533

CALCULATION OF TOTAL FEES DUE						
CLAIMS FEES	Number Filed (Col. 1)	No. Extra (Col. 2)	Small Entity		Large Entity	
			Rate ($)	Fee ($)	Rate ($)	Fee ($)
Basic Fee				385		770
Total Claims	3 - 20 =	0	x 11 =		x 22 =	0
Indep. Claims	2 - 3 =	0	x 40 =	0	x 80 =	0
[ ] Multiple dependent claim presented *If the difference in Col. 1 is less than zero, enter "0" in Col. 2			x 130 =		x 260 =	
TOTAL APPLICATION FEES						770
An extension of a shortened statutory time for response under 37 CFR 1.136(a) is requested as indicated below or as necessary to maintain the pendency of the priority application						
Extension Fees	1 Month 2 Months 3 Months 4 Months		$ 55.00 195.00 465.00 735.00		$ 110.00 390.00 930.00 1,470.00	
Any Other Fees:						
[ ] Assignment Recording Fee (Recordation Form Cover Sheet included)						
TOTAL FEES SUBMITTED						770

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

priority Application Serial No. 08/582,385
priority Filing Date . . . . . January 3, 1996
Inventor . . . . . G. Sandhu
Assignee . . . . . Micron Technology, Inc.
priority Group Art Unit 2109
Examiner . . . . . unknown
Attorney's Docket No. MI22-713
Title: Capacitor Constructions (As amended)

REQUEST FOR DIVISIONAL APPLICATION UNDER RULE 1.60(b)

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99204-0317

Sir:

This is a request for filing a divisional application under 37 CFR §1.60(b) of prior application Serial No. 08/582,385, filed on January 3, 1996, entitled "Capacitor Constructions (As Amended)" by the following named inventors: Gurtej S. Sandhu, 2964 E. Parkriver Drive, Boise, ID 83706; and Pierre C. Fazan, Riant Coin 32 1093 LA, Conversion, Switzerland SC208.

No abandonment or termination of proceedings has occurred in the above-identified prior application.

The above identified prior application is a complete application as set forth in 37 CFR §1.51(a).

[X] 1. A Preliminary Amendment is enclosed.

[X] 2. The filing fee of $770 is enclosed calculated on the basis of the claims existing in the prior application as presently amended.

[X] 3. The Commissioner is hereby authorized to charge fees under 37 CFR §1.16 and §1.17 associated with this communication, or credit any overpayment to Deposit Account No. 23-0925.

[X] 4. The Commissioner is hereby authorized to charge payment of the following fees during pendency of this application or credit any overpayment to Deposit Account No. 23-0925; any patent application processing fees under 37 CFR §1.17; any filing fees under 37 CFR §1.16 for presentation of additional claims.

[X] 5. The filing date of pending application Serial No. 08/582,385 is hereby claimed under 35 U.S.C. §120.

[X] 6. The prior application is assigned of record to Micron Technology, Inc. Such assignment is effective for this application, and is recorded starting at Reel 7828, Frame 0461.

[X] 7. The power of attorney in the prior application appoints the following attorneys and agents for which authority is still effective: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268;

James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen, Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G. Grigel, Reg. No. 31,166; Keith D. Gzelak, Reg. No. 37,144; and John S. Reid, Reg. No. 36,369.

[X] 8. Information Disclosure Statement with form PTO-1449 is enclosed.

Address all future correspondence to: WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane, WA 99204-0317. Direct telephone calls to: David G. Latwesen (509) 624-4276.

The undersigned states that a true copy of the prior complete application as filed is enclosed, including the specification, claims, drawings, oath or declaration showing applicant's signature, and any amendments referred to in the oath or declaration to complete the prior application.

Respectfully submitted,

Dated: 2/1/97 By: _____

David G. Latwesen, Ph.D.
Reg. No. 38,533

Attorneys for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

priority Application Serial No. 08/582,385
priority Filing Date . . . . . January 3, 1996
Inventor . . . . . G. Sandhu
Assignee . . . . . Micron Technology, Inc.
priority Group Art Unit 2109
Examiner . . . . . unknown
Attorney's Docket No. MI22-713
Title: Capacitor Constructions (As amended)

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99204-0317

AMENDMENTS

In the Specification

Replace the title with --Capacitor Constructions--.

At page 1, before the "Technical Field" section, insert --**RELATED PATENT DATA**

This patent resulted from a divisional application of United States Patent Application Serial No. 08/582,385, which was filed January 3, 1996, titled "Capacitor Constructions", and listed the inventors as Gurtej Sandhu and Pierre C. Fazan.--

Amended Claims

Cancel claims 1-42.

REMARKS

Claims 1-42 are canceled, leaving claims 43-45 pending in the application. Applicant requests examination of claims 43-45.

Respectfully submitted,

Dated: 2/11/97 By: _____

David G. Latwesen, Ph.D.
Reg. No. 38,533

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Method Of Forming A Capacitor And A Capacitor Construction

* * * * *

INVENTORS:

Gurtej Sandhu
Pierre C. Fazan

ATTORNEY'S DOCKET NO. MI22-415

TECHNICAL FIELD

This invention relates generally to capacitor formation in semiconductor wafer processing, and to resultant capacitor constructions.

BACKGROUND OF THE INVENTION

As DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell area. Additionally, there is a continuing goal to further decrease cell area.

The principal way of increasing cell capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors, such as trenched or stacked capacitors. This invention concerns stacked capacitor cell constructions, including what are commonly known as crown or cylindrical container stacked capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 9.

Fig. 11 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a diagrammatic sectional view of an alternate embodiment semiconductor wafer fragment at a processing step in accordance with the invention.

Fig. 14 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that shown by Fig. 14.

Fig. 16 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a diagrammatic sectional view of another alternate embodiment semiconductor wafer fragment at a processing step in accordance with the invention.

Fig. 18 is a view of the Fig. 17 wafer fragment at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a view of the Fig. 17 wafer fragment at a processing step subsequent to that shown by Fig. 18.

Fig. 20 is a view of the Fig. 17 wafer fragment at a processing step subsequent to that shown by Fig. 19.

Fig. 21 is a view of the Fig. 17 wafer fragment at a processing step subsequent to that shown by Fig. 20.

Fig. 22 is a diagrammatic sectional view of yet another alternate embodiment semiconductor wafer fragment at a processing step in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a method of forming a capacitor comprises the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

after providing the node, providing a finned lower capacitor plate in ohmic electrical connection with the node using no more than one photomasking step; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

In accordance with another aspect of the invention, a method of forming a capacitor comprises the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

providing a layer of conductive material outwardly of the node;

providing a first masking layer over the conductive material layer;

etching a first opening into the first masking layer over the node;

providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening;

anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second

opening relative to the first masking layer which is smaller than the first opening;

after anisotropically etching the second masking layer, etching unmasked first masking layer material away;

after anisotropically etching the second masking layer, etching through the conductive material layer to extend the second opening to the node, the node and conductive layer being electrically isolated from one another after the conductive material layer etching;

plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and conductive layer; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

Referring to Fig. 1, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a bulk monocrystalline silicon substrate 12 having diffusion regions 13, 14, 15 provided therein. A pair of word lines 16 and 17 are provided as shown. Such comprise a gate oxide region 18, a polysilicon conductive region 19, a higher conductivity silicide region 20, and an electrically insulative oxide or nitride cap 21. An etch stop layer 22 is provided, to an example thickness of 500 Angstroms. A preferred material for layer 22 is Si_3N_4, the optional use of which will be apparent subsequently.

Referring to Fig. 2, an insulating dielectric layer 24 is provided over etch stop layer 22. Such is planarized, and a storage node contact 25 opened therethrough to outwardly expose diffusion region 14.

Referring to Fig. 3, a layer of conductive material is deposited and planarized back relative to oxide layer 24 to define a pillar 26 which projects from diffusion region 14 provided in bulk semiconductive substrate 12. For purposes of the continuing discussion, pillar 26 comprises an outer surface 28 which constitutes a node to which electrical connection to a first capacitor plate is to be made. An example preferred plugging material 26 is conductively doped polysilicon.

Referring to Fig. 4, a plurality of alternating first layers 30 and second layers 32 are provided outwardly relative to node 28. Example and preferred thicknesses for layers 30 and 32 are from 200 Angstroms to 700 Angstroms. The material of first layers 30 is chosen to be selectively etchable relative to node 28, and also to material of second layer 32. An example and preferred material for layers 30 is undoped SiO_2 deposited by decomposition of tetraethylorthosilicate (TEOS). Second layer material 32 is chosen to be selectively etchable relative to first layer material 30 and also be electrically conductive. An example and preferred material for layer 32 is conductively doped polysilicon, with the material of layer 32 and plugging material 26 in the preferred embodiment thereby constituting the same material. Further, the first layer material 30 is preferably entirely sacrificial, but nevertheless preferably constitutes an electrically insulative material. The alternating

stack of first and second layers 30 and 32 are shown as terminating in an upper layer 30, although an upper layer 32 could ultimately be provided.

Referring to Fig. 5, a first masking layer 34 is provided over the alternating layers 30 and 32, and thus over and outwardly relative to second layer material 32. In the described and preferred embodiment a plurality of alternating layers 30 and 32 are provided for production of a multi-finned capacitor construction as will be apparent subsequently. In accordance with one alternate aspect of the invention, only a single first layer 30 and a single second layer 32 might be utilized. A first opening 35 is etched into first masking layer 34 over node 28. An example and preferred material for layer 34 is a doped oxide deposited to an example thickness of 2,000 Angstroms.

Referring to Fig. 6, a second masking layer 36 is provided over first masking layer 34 to a thickness which less than completely fills first opening 35. An example and preferred material for layer 36 is Si_3N_4.

Referring to Fig. 7, second masking layer 36 is anisotropically etched to define a spacer 38 received laterally within first opening 35, and thereby defining a second opening 39 relative to first masking layer 34 which is smaller than first opening 35.

Referring to Fig. 8, unmasked first layer material 34 has been etched away. An example etch for stripping layer 34 where it comprises borophosphosilicate glass (BPSG), layer 30 comprises undoped

SiO_2 and spacer 38 comprises Si_3N_4 comprises a wet etch with a HF solution.

Referring to Fig. 9, and with spacer 38 in place, the alternating layers 30 and 32 are etched as shown to define a desired outline (as will be apparent subsequently) of a first capacitor plate and to extend second opening 39 through such alternating layers to node 28. Such etching is preferably conducted for both layers to be highly anisotropic as shown and conducted such that each alternating etch is selective relative to the immediate underlying layer. During such collective etching, spacer 38 constitutes an etching mask. Where spacer 38 comprises Si_3N_4, layers 30 comprise undoped SiO_2, and layers 32 comprise conductively doped polysilicon, an example etch which will remove such oxide selectively relative to the nitride and polysilicon is using a fluorine and hydrocarbon plasma chemistry which is preferably carbon rich. For the same materials, an example etch which will anisotropically and selectively remove polysilicon of layer 32 anisotropically and selectively relative to nitride and SiO_2 is chlorine and HBr plasma.

Such etching effectively defines the illustrated etched layers 32 to constitute a plurality of laterally projecting electrically conductive first capacitor plate fins. The illustrated etch stopping effect relative to insulating layer 24 will not occur where the material of first layers 30 and layer 24 are the same, but will occur where the etch characteristics

of layers 30 and 24 can be conducted differently relative to one another.

Referring to Fig. 10, spacer 38 has been etched away, and an electrically conductive plugging material 44 provided within second opening 39. Accordingly, plugging material 44 electrically interconnects node 28 with the illustrated plurality of second layers/fins 32. An example and preferred technique for providing such layer is to deposit a polycrystalline layer to fill the void and subsequently conduct an anisotropic polycrystalline etch selective to oxide using chlorine and HBr plasma chemistry. Thus in a most preferred embodiment, the material of node 28, plugging material 44 and second layer material 32 all constitute the same material.

Referring to Fig. 11, first layer material 30 is selectively isotropically etched relative to second layer material 32. Preferably, the material of layers 30 and 24 constitutes the same material such that etching of layer 24 also occurs, with etch stop layer 22 acting as an etch stop relative to the word lines and bulk substrate as shown. Where layers 24 and 30 constitute undoped SiO_2, an example etching chemistry is an HF solution. The preferred result is the illustrated multi, horizontally finned lower capacitor plate 50 which is effectively in ohmic electrical connection relative the node 28.

Referring to Fig. 12, a capacitor dielectric layer 52 and a subsequent electrically conductive second capacitor plate layer 54 are provided over the illustrated conductive second layers/fins 32 of first

capacitor plate 50. This constitutes but one example of forming a capacitor utilizing no more than one photomasking step in producing a finned (preferably multi finned) lower capacitor plate in ohmic electrical connection after providing a node for connection thereto.

In contradistinction to the prior art, only one photomasking step (that to form first opening 35) has been utilized to define all of first capacitor plate 50 between the step of providing node 28 and subsequent steps wherein capacitor dielectric and second conductive plates are provided. Further, the stem/plug 44 diameter can be provided to be less than the minimum photolithograpic feature size/dimension due to the maskless anisotropic etch by which the void for the plug is formed. Thus, more of the available capacitor volume can be consumed by surface-area-enhancing fins than from the stem or plug 44.

An example alternate embodiment is described with reference to Figs. 13-16. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals. Fig. 13 illustrates a wafer fragment 10a at a processing step immediately subsequent to that depicted by Fig. 8 in the first described embodiment. Here, a third masking layer 60 is provided over spacer 38. Layer 60 can be the same as or different from the material of layer 38.

Referring to Fig. 14, third masking layer 60 is anisotropically etched to form a secondary spacer 62 laterally outward of first stated spacer 38.

Referring to Fig. 15, spacers 62 and 38 are used collectively as an etching mask during the second and first layer etchings to produce the modified construction which extends considerably further laterally outward beyond the boundaries of the first described embodiment capacitor. The same above example etch chemistries can be utilized for effecting the Fig. 15 etch construction where layer 62 comprises BPSG.

Referring to Fig. 16, spacers 62 and 38 etched away, polysilicon plugging material 44 is provided, and first layers 30 are isotropically etched, thus resulting in the modified illustrated first capacitor plate construction 50a.

The above described alternate processing enables placement of adjacent capacitors of a DRAM array closer to one another than the minimum available photolithographic feature size. Prior art processing typically provides the closest spacing between adjacent capacitor edges as being the minimum available photolithographic feature width. In accordance with the above described alternate preferred embodiment, closer placement of such capacitor edges may be possible due to the outer capacitor plate edge being defined by a photolithographic feature at its minimum feature. Accordingly, the mask utilized to produce the mask opening which produces the first corresponding opening of the adjacent capacitor can be placed closer to the edge of the adjacent

opening of the described and illustrated capacitor. Such is shown by way of example in Fig. 22 with respect to a wafer fragment 10c. A pair of finned capacitors 50a and 50c are shown separated by a spacing "s", which can be less than the minimum available photolithographic feature size.

Yet another alternate embodiment method is described with reference to Figs. 17 - 21. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by the suffix "b" or with different numerals. Fig. 17 is the same as Fig. 6, but for provision of an additional masking layer 70 over first masking layer 34. Layer 70 is preferably provided where layers 30 and 34 constitute the same material, as will be apparent from Fig. 18. As there shown, anisotropic etching of second masking layer 36 has occurred to form second opening 39, with subsequent etching of layers 30 and 32 having been conducted to extend such opening to node 28. During such extension etching, layer 34 remains in place with additional masking layer 70 restricting etching of layer 34 while layers 30 are being etched.

Referring to Fig. 19, a conductive plugging layer 44b is deposited. Referring to Fig. 20, layer 44b is etched or planarized back as shown, and masking layers 70 and 34 also etched. Referring to Fig. 21, layers 30 and 32 are etched to define the capacitor outline, with plugging material 44b also being etched in the process where it is provided to be the same material as layers 32. Thus in this described

embodiment, the unmasked first masking layer is etched after extending the second opening to the node where in the first described embodiment it is conducted before.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

providing a first layer of material over the node, the first layer of material being selectively etchable relative to the node;

providing a second layer of material over the first layer, the second layer of material being selectively etchable relative to the first layer of material and being electrically conductive;

providing a first masking layer over the second layer of material;

etching a first opening into the first masking layer over the node;

providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening;

anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second opening relative to the first masking layer which is smaller than the first opening;

after anisotropically etching the second masking layer, etching unmasked first masking layer material away;

after anisotropically etching the second masking layer, selectively anisotropically etching the second layer of material relative to the first layer of material;

after etching the second layer material, selectively etching the first layer of material relative to the node to effectively extend the second opening to the node and define an outline of the first capacitor plate using the spacer as an etching mask;

plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and second layer;

after extending the second opening to the node, selectively isotropically etching the first layer material relative to the second layer material; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive second layer.

2. The method of forming a capacitor of claim 1 wherein the first opening is provided to have a minimum opening width equal to the minimum capable photolithographic feature dimension at the time of fabrication, the second opening thereby having a minimum opening width which is less than the minimum capable photolithographic feature dimension at the time of fabrication, the resultant plugging material plugging the second opening thereby having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

3. The method of forming a capacitor of claim 1 wherein the unmasked first masking layer is etched before extending the second opening to the node.

4. The method of forming a capacitor of claim 1 wherein the unmasked first masking layer is etched after extending the second opening to the node.

5. The method of forming a capacitor of claim 1 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

6. The method of forming a capacitor of claim 1 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

7. The method of forming a capacitor of claim 1 wherein the first layer is electrically insulative.

8. The method of forming a capacitor of claim 1 wherein the first layer predominately comprises SiO_2.

9. The method of forming a capacitor of claim 1 wherein the second layer material constitutes the same material as that of the node.

10. The method of forming a capacitor of claim 1 wherein the plugging material, the node and the second layer of material all constitute the same material.

11. The method of forming a capacitor of claim 1 wherein the second masking material comprises Si_3N_4.

12. The method of forming a capacitor of claim 1 further comprising after selectively etching the first layer, etching the spacer away.

13. The method of forming a capacitor of claim 1 wherein the step of selectively etching the first layer comprises anisotropically etching the first layer.

14. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; and

the first layer is electrically insulative.

15. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate;

the first layer is electrically insulative; and

further comprising after selectively etching the first layer, etching the spacer away.

16. The method of forming a capacitor of claim 1 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate;

the first layer is electrically insulative;

further comprising after selectively etching the first layer, etching the spacer away; and

wherein the plugging material, the node and the second layer of material all constitute the same material.

17. The method of forming a capacitor of claim 1 comprising etching the first masking layer away before anisotropically etching the second layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

18. The method of forming a capacitor of claim 17 further comprising forming at least two of said capacitors, the two capacitors being adjacent one another and having a minimum spacing from one another which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

19. The method of forming a capacitor of claim 1 further comprising providing a plurality of alternating of the first and second layers outwardly relative to the node, and providing the first and second masking layers and first and second openings outwardly thereof;

the method further comprising alternatingly anisotropically etching the respective second and first layers to extend the second opening therethrough to the node; and

the step of isotropically etching the first layer material relative to the second layer material defining a plurality of laterally projecting electrically conductive second layer fins.

20. The method of forming a capacitor of claim 19 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

21. The method of forming a capacitor of claim 19 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

22. The method of forming a capacitor of claim 19 wherein the first layer is electrically insulative.

23. The method of forming a capacitor of claim 19 wherein the plugging material, the node and the second layer material all constitute the same material.

24. The method of forming a capacitor of claim 19 further comprising after selectively etching the first layer, etching the spacer away.

25. The method of forming a capacitor of claim 19 comprising etching the first masking layer away before anisotropically etching the second layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

26. The method of forming a capacitor of claim 19 wherein,

the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; and

the first layer is electrically insulative.

27. The method of forming a capacitor of claim 19 wherein, the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; the first layer is electrically insulative; and

further comprising after selectively etching the first layer, etching the spacer away.

28. The method of forming a capacitor of claim 19 wherein, the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate; the first layer is electrically insulative;

further comprising after selectively etching the first layer, etching the spacer away; and

wherein the plugging material, the node and the second layer of material all constitute the same material.

29. A capacitor produced according to the method of claim 1.

30. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

providing a layer of conductive material outwardly of the node;

providing a first masking layer over the conductive material layer;

etching a first opening into the first masking layer over the node;

providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening;

anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second opening relative to the first masking layer which is smaller than the first opening;

after anisotropically etching the second masking layer, etching unmasked first masking layer material away;

after anisotropically etching the second masking layer, etching through the conductive material layer to extend the second opening to the node, the node and conductive layer being electrically isolated from one another after the conductive material layer etching;

plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and conductive layer; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

31. The method of forming a capacitor of claim 30 wherein the first opening is provided to have a minimum opening width equal to the minimum capable photolithographic feature dimension at the time of fabrication, the second opening thereby having a minimum opening width which is less than the minimum capable photolithographic feature dimension at the time of fabrication, the resultant plugging material plugging the second opening thereby having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

32. The method of forming a capacitor of claim 30 wherein only one photomasking step is utilized to define the first capacitor plate between the step of providing the node and the step of providing the capacitor dielectric layer.

33. The method of forming a capacitor of claim 30 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

34. The method of forming a capacitor of claim 30 wherein the conductive material layer constitutes the same material as that of the node.

35. The method of forming a capacitor of claim 30 wherein the plugging material, the node and the conductive material layer all constitute the same material.

36. The method of forming a capacitor of claim 30 wherein the second masking material comprises Si_3N_4.

37. The method of forming a capacitor of claim 30 further comprising after etching through the conductive material layer, etching the spacer away.

38. The method of forming a capacitor of claim 30 comprising etching the first masking layer away before etching through the conductive layer material, and then further comprising:

providing a third masking layer over the spacer;

anisotropically etching the third masking layer to form a secondary spacer laterally outward of the first stated spacer; and

using said spacers collectively as an etching mask during the second and first layer etchings.

39. A capacitor produced according to the method of claim 30.

40. A method of forming a capacitor comprising the following steps:

providing a node to which electrical connection to a first capacitor plate is to be made;

after providing the node, providing a finned lower capacitor plate in ohmic electrical connection with the node using no more than one photomasking step; and

providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer.

41. The method of forming a capacitor of claim 40 wherein the node comprises an outer surface of a pillar which projects from a diffusion region provided in a bulk semiconductive substrate.

42. The method of forming a capacitor of claim 40 wherein the finned lower capacitor plate constitutes the same material as that of the node.

43. A capacitor construction comprising:

a stem; and

at least two laterally opposed fins interconnected with and projecting laterally from the stem, the stem having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

44. A pair of adjacent capacitors fabricated relative to a semiconductor substrate, the adjacent capacitors having a minimum lateral spacing from one another which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

45. The capacitors of claim 44 wherein each comprises:

a stem; and

at least two laterally opposed fins interconnected with and projecting laterally from the stem, the stem having a minimum width which is less than the minimum capable photolithographic feature dimension at the time of fabrication.

ABSTRACT OF THE DISCLOSURE

A method of forming a capacitor includes, a) providing a node to which electrical connection to a first capacitor plate is to be made; b) then, providing a finned lower capacitor plate in ohmic electrical connection with the node using no more than one photomasking step; and c) providing a capacitor dielectric layer and a conductive second capacitor plate layer over the conductive layer. Such is preferably accomplished by, i) providing a layer of conductive material outwardly of the node; ii) providing a first masking layer over the conductive material layer; iii) etching a first opening into the first masking layer over the node; iv) providing a second masking layer over the first masking layer to a thickness which less than completely fills the first opening; v) anisotropically etching the second masking layer to define a spacer received laterally within the first opening and thereby defining a second opening relative to the first masking layer which is smaller than the first opening; vi) after said anisotropically etching, etching unmasked first masking layer material away; vii) after said anisotropically etching, etching through the conductive material layer to extend the second opening to the node, the node and conductive layer being electrically isolated from one another after the conductive material layer etching; viii) plugging the extended second opening with an electrically conductive plugging material, the plugging material electrically interconnecting the node and conductive layer. Novel capacitor constructions are also disclosed.

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Method Of Forming A Capacitor And A Capacitor Construction,** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen,

Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G. Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; and John S. Reid, Reg. No. 36,369.

Send correspondence to: WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane, WA 99204-0317. Direct telephone calls to: Mark S. Matkin, (509) 624-4276.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of inventor: **Gurtej Sandhu**

Inventor's Signature: _____

Date: 12/22/95

Residence: **Boise, Idaho**

Citizenship: **United Kingdom**

Post Office Address: **2964 E. Parkriver Drive**
Boise, ID 83706

* * * * * * * * * * *

Full name of inventor: **Pierre C. Fazan**

Inventor's Signature: Pierre Fazan

Date: 12/22/95

Residence: **Boise, Idaho**

Citizenship: **Switzerland**

Post Office Address: **2267 Illinois Avenue**
Boise, ID 83706

AS FILED

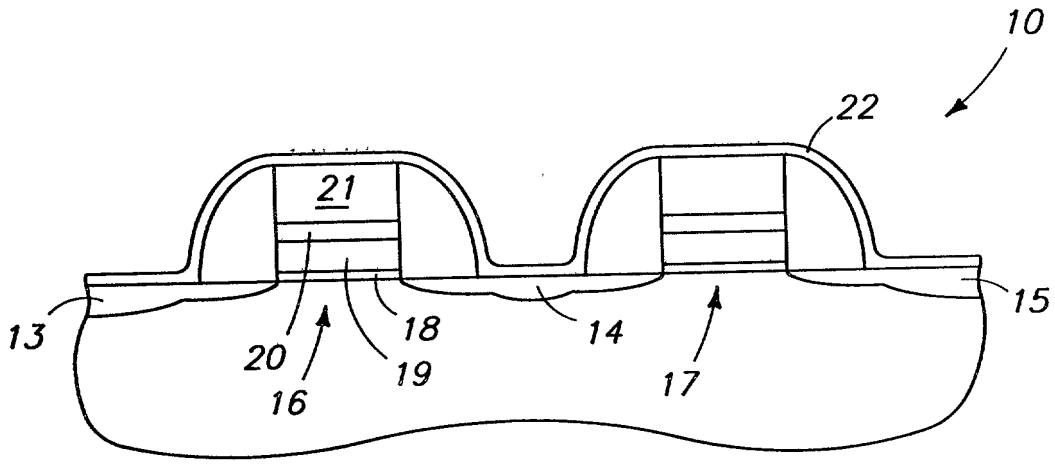

Fig 1

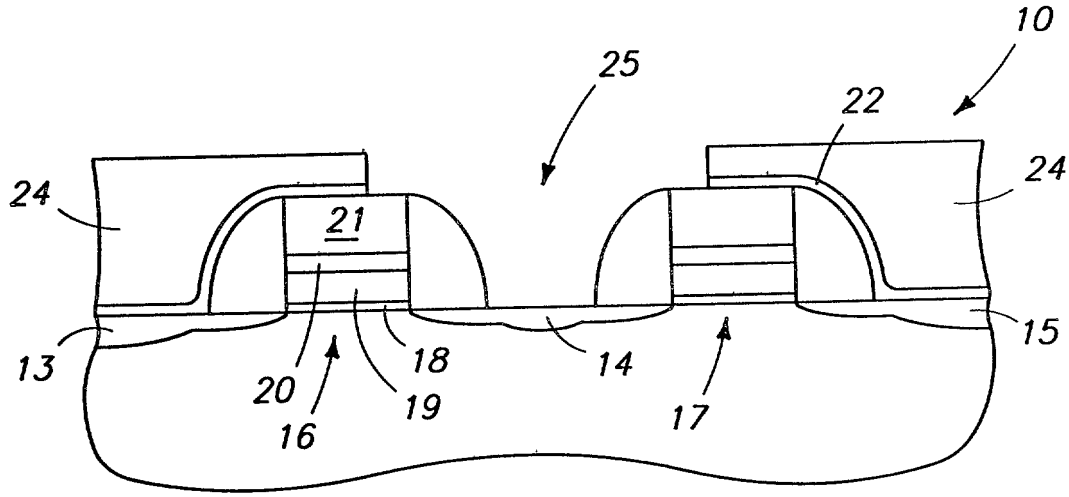

Fig 2

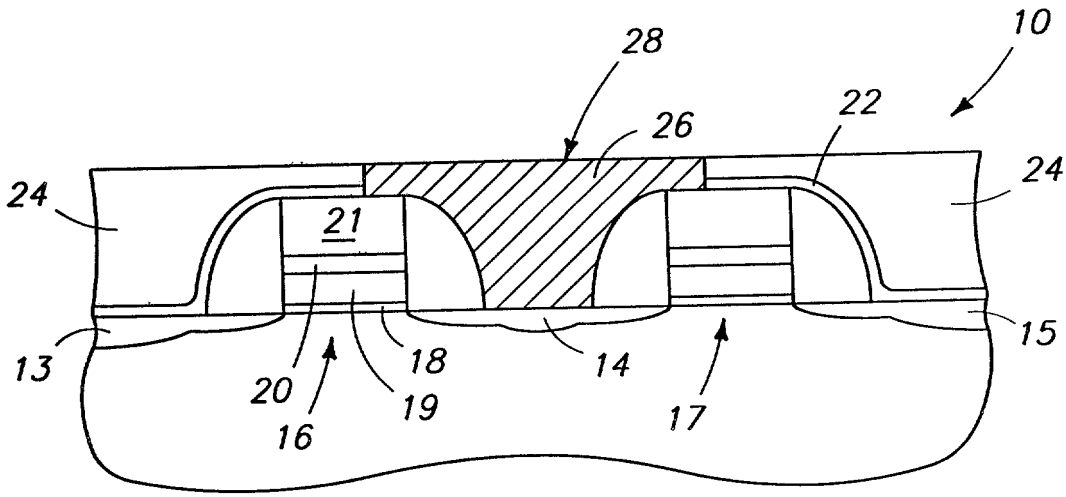

Fig 3

AS FILED

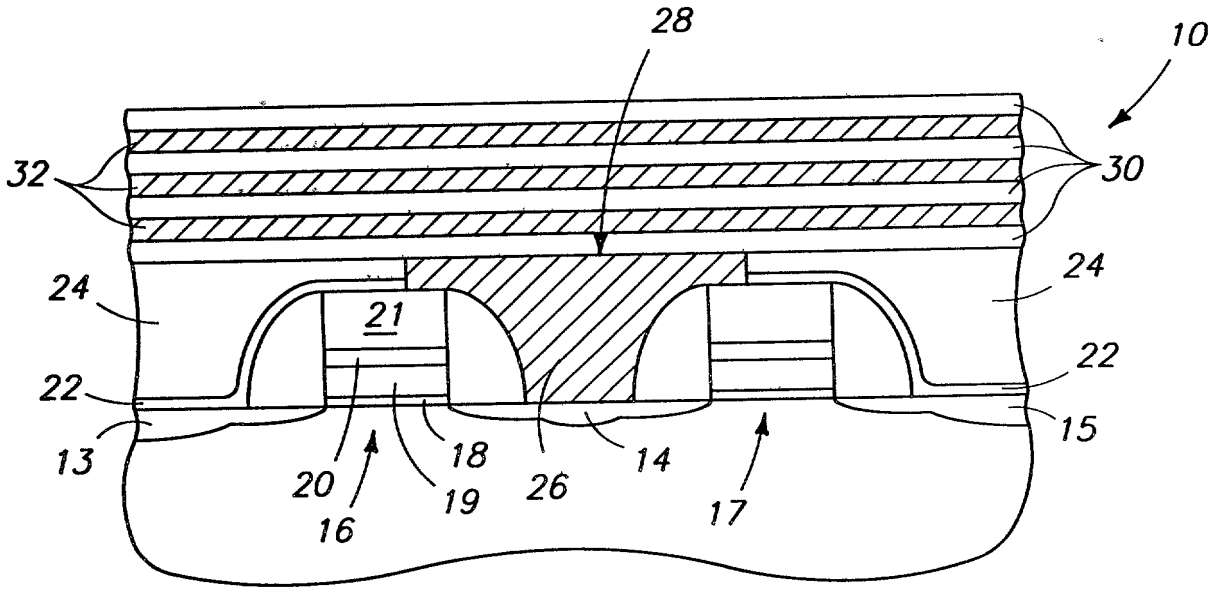

Fig 4

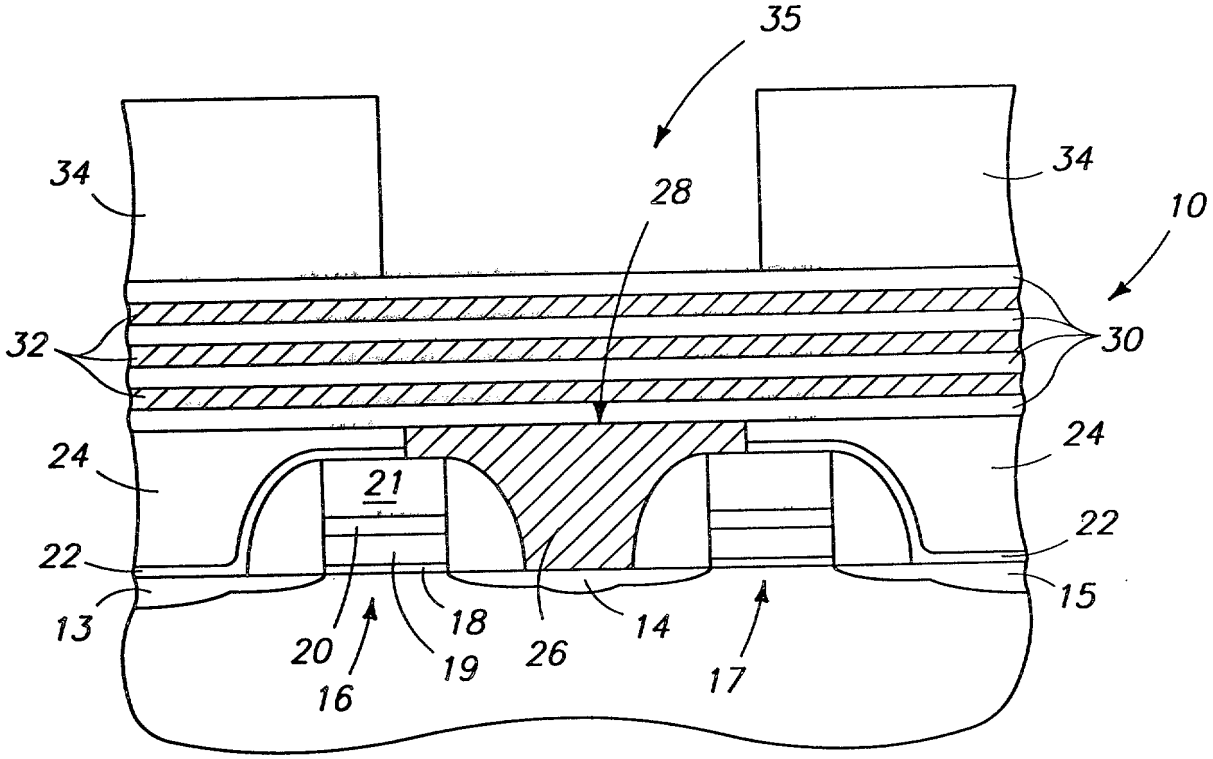

Fig 5

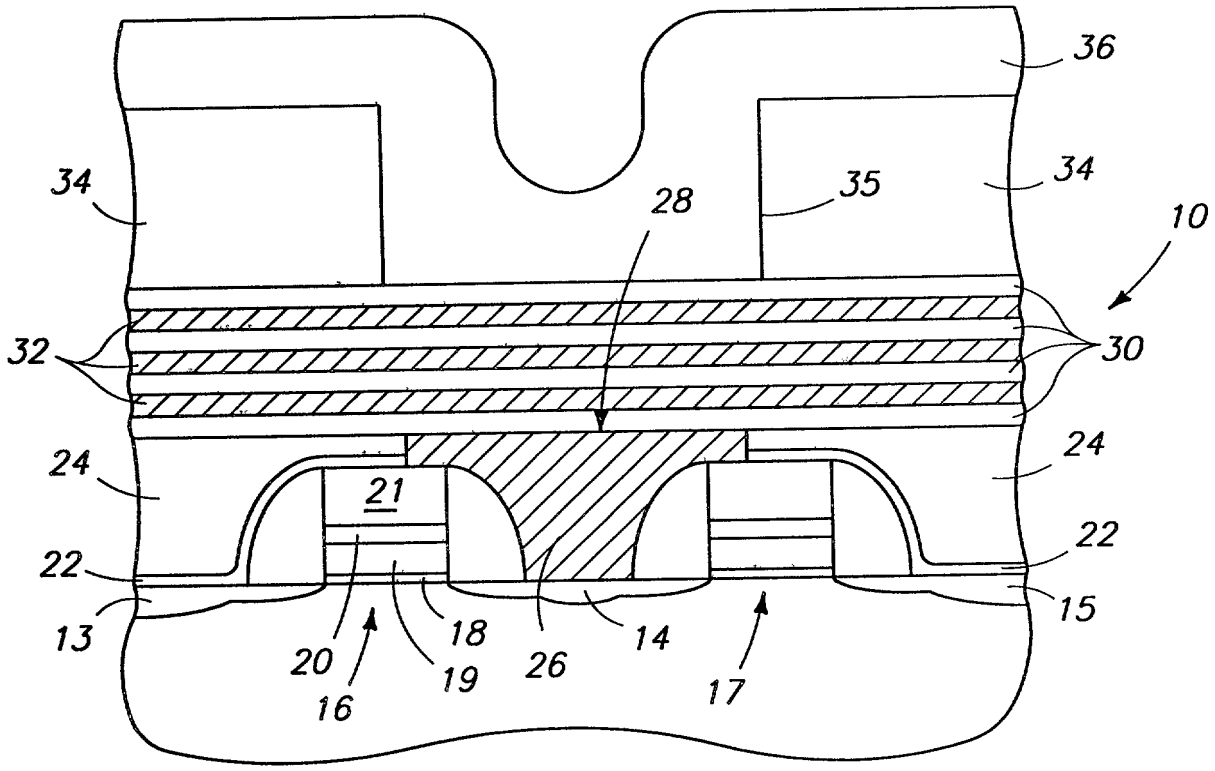

Fig 6

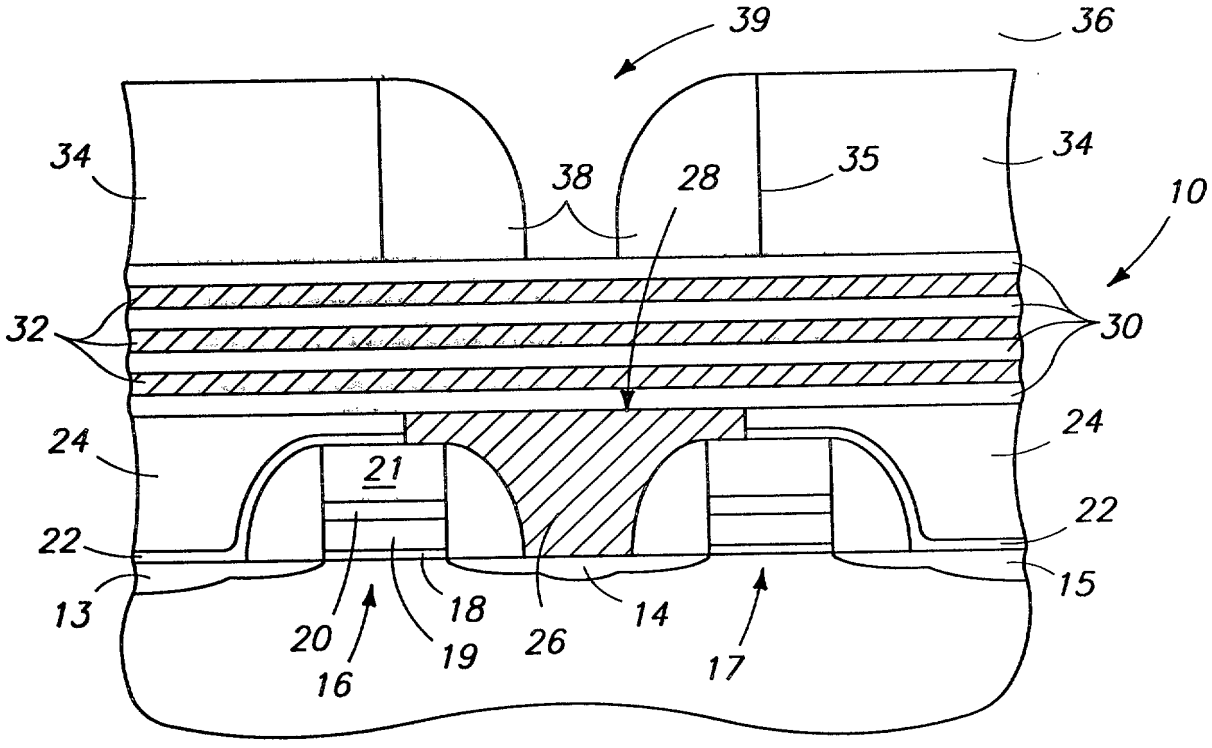

Fig 7

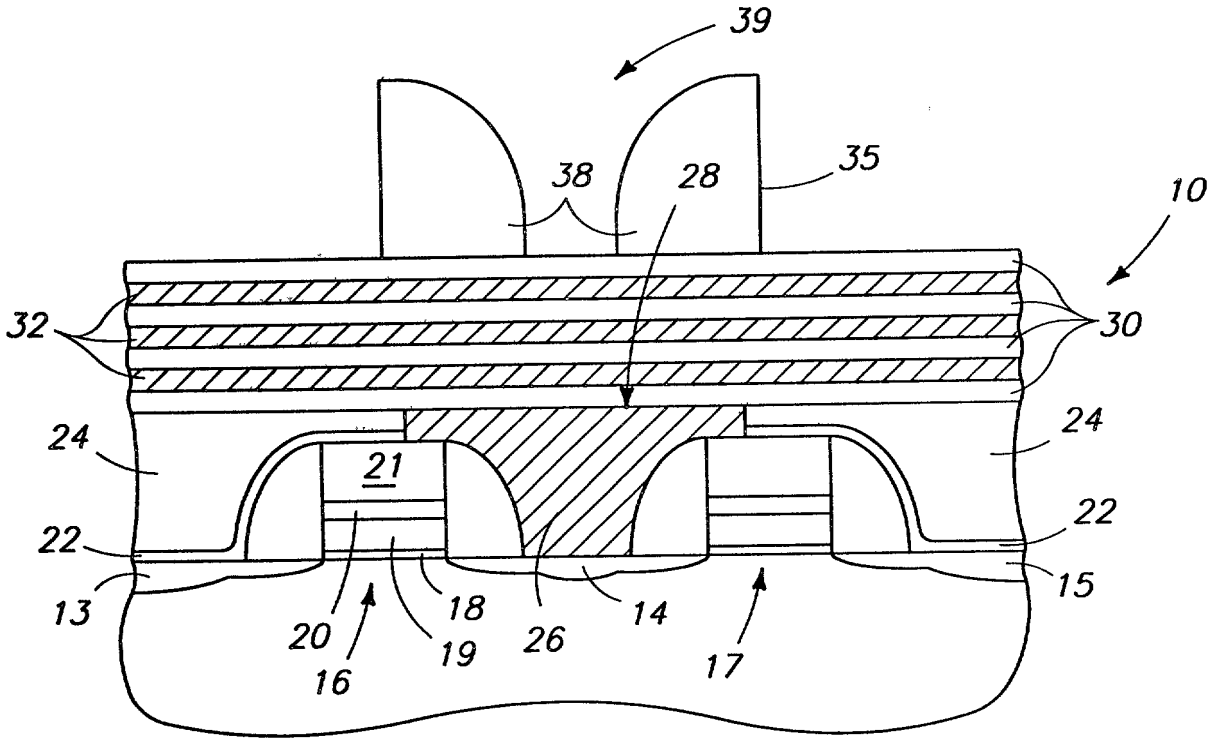

Fig 8B

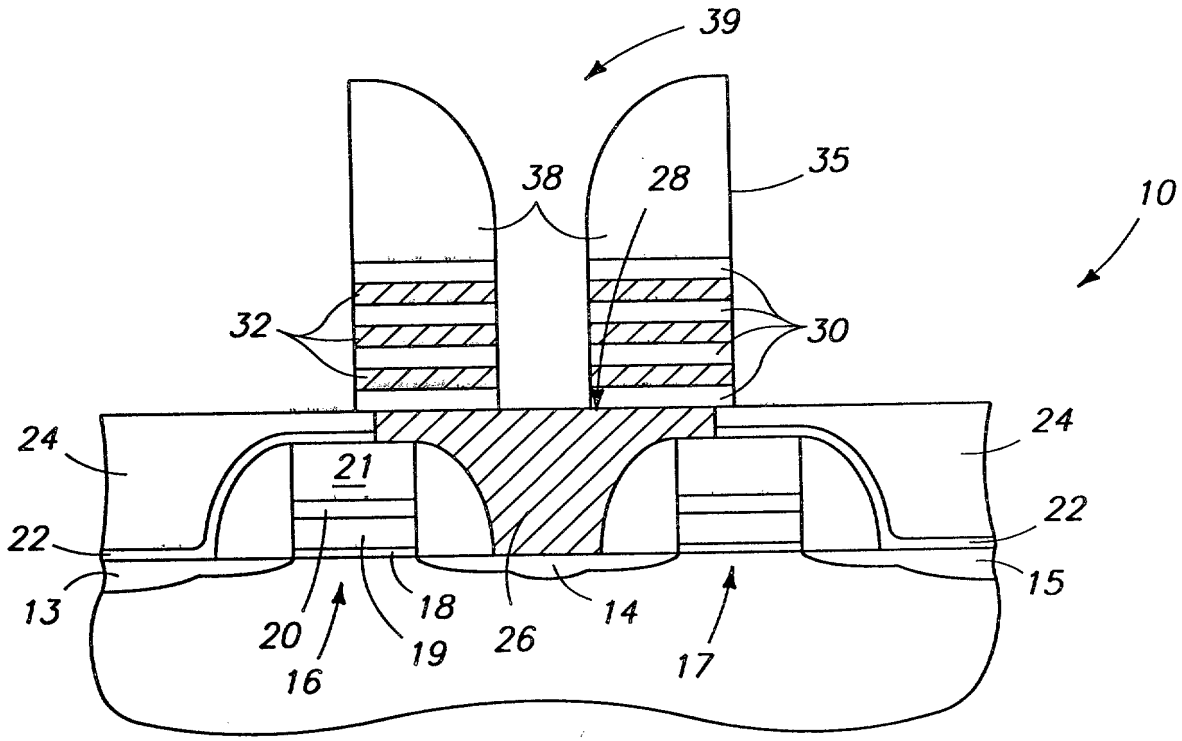

Fig 9

AS FILED

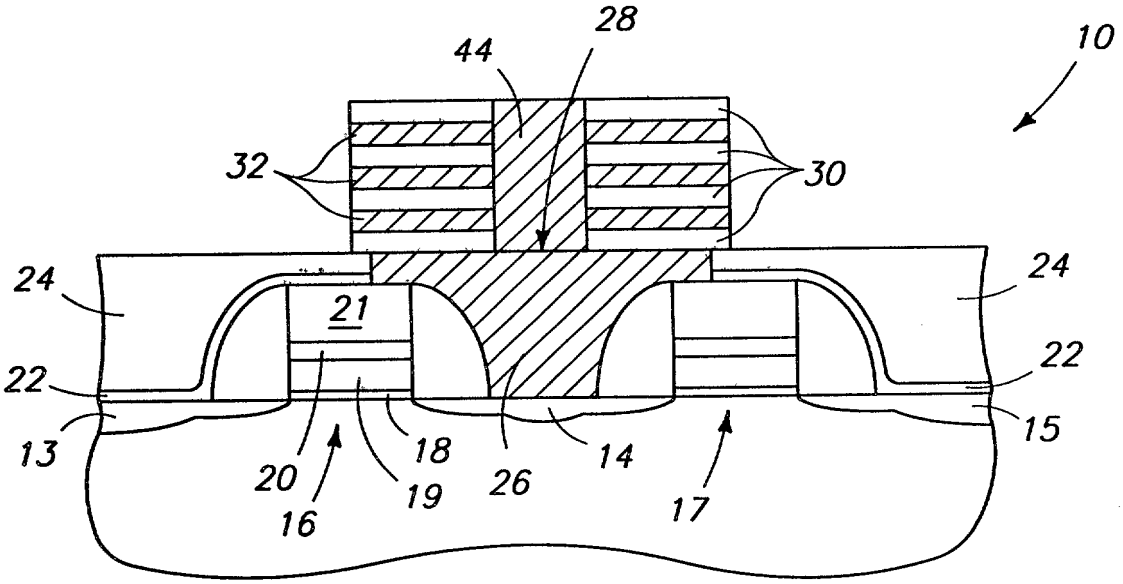

Fig. 3

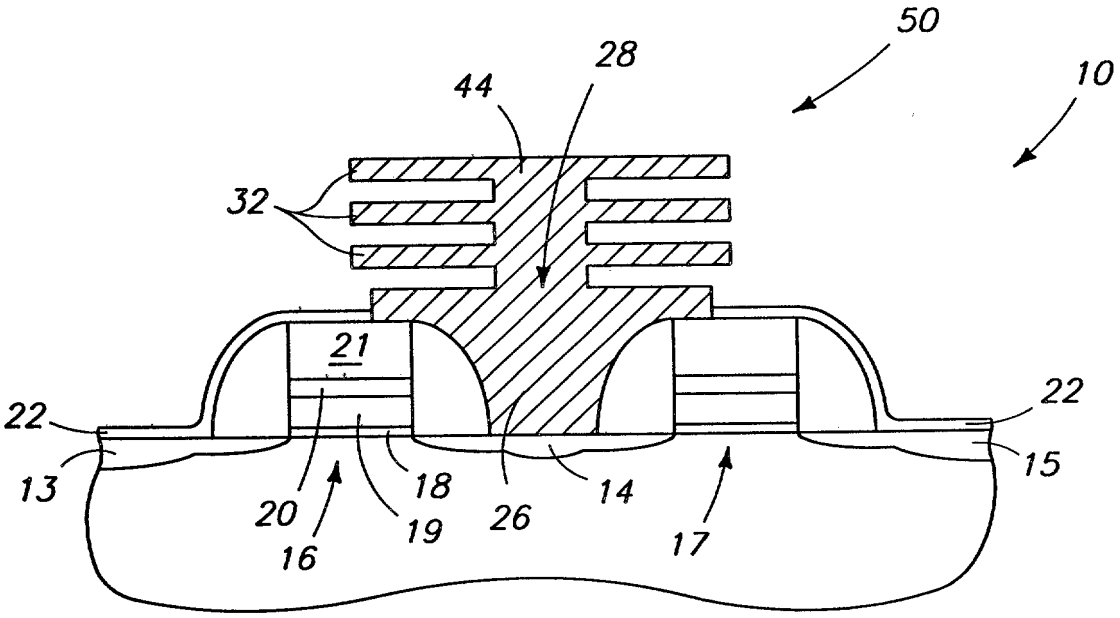

Fig. 2

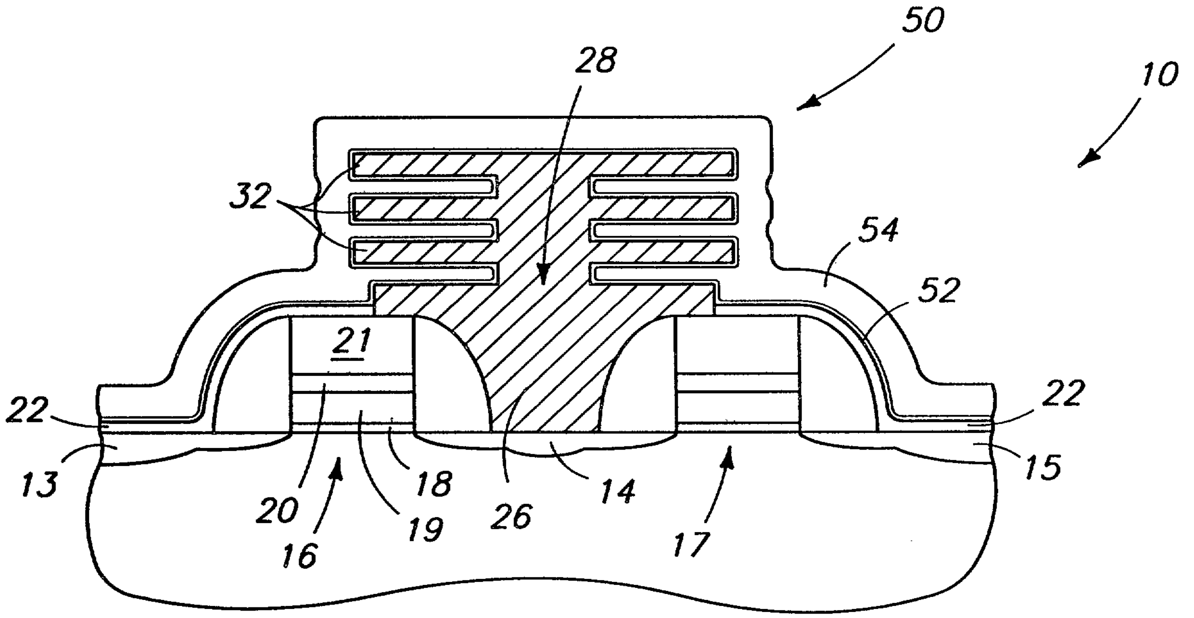

Fig 12

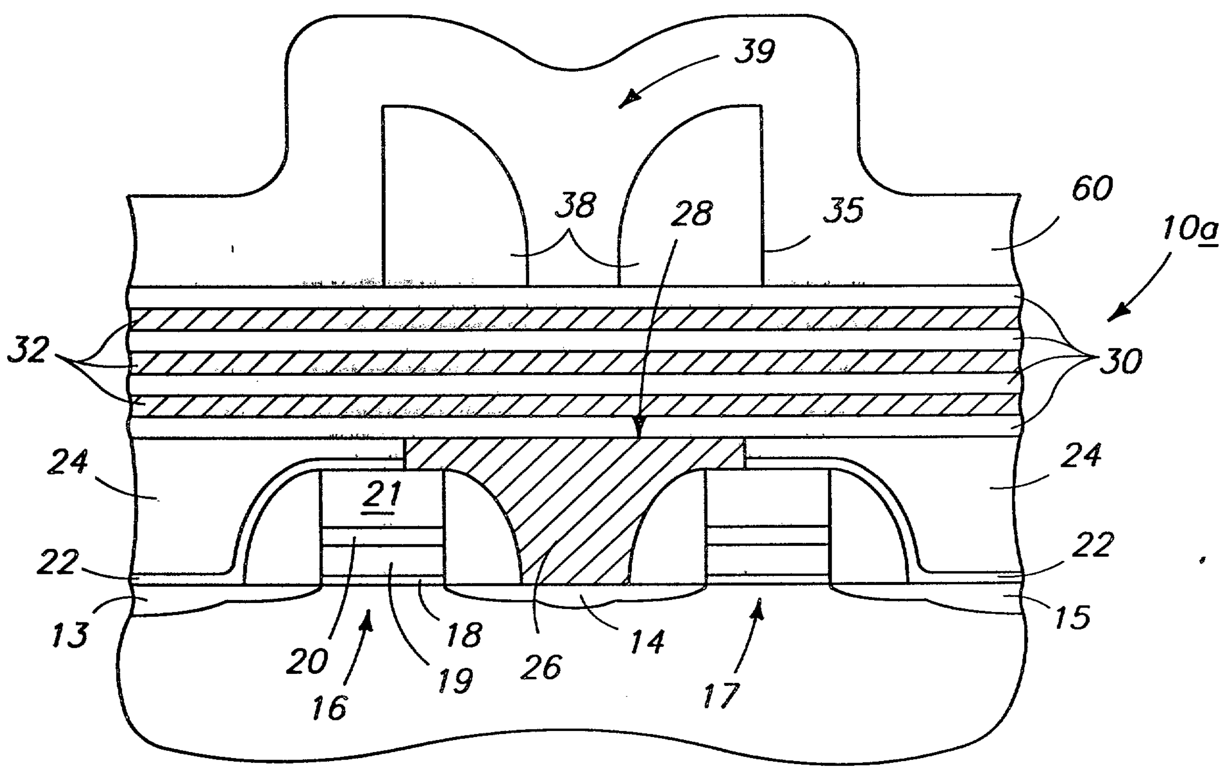

Fig 13

AS FILED

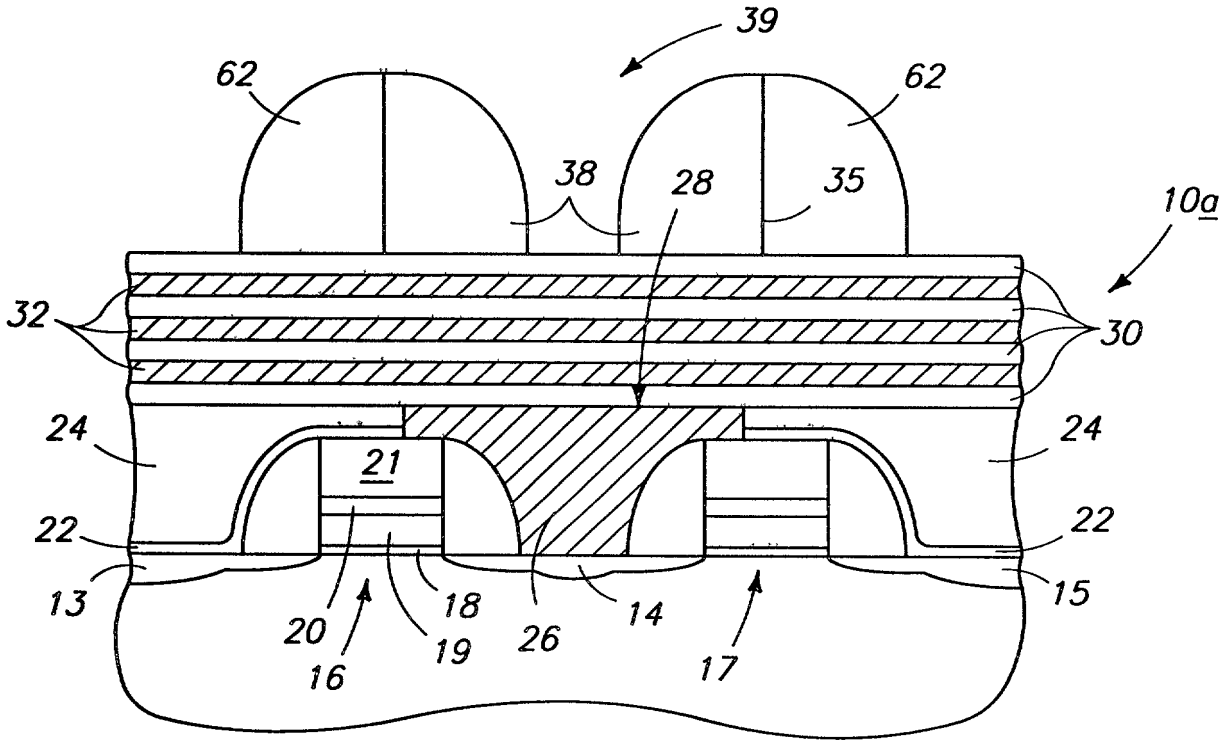

Fig. 14

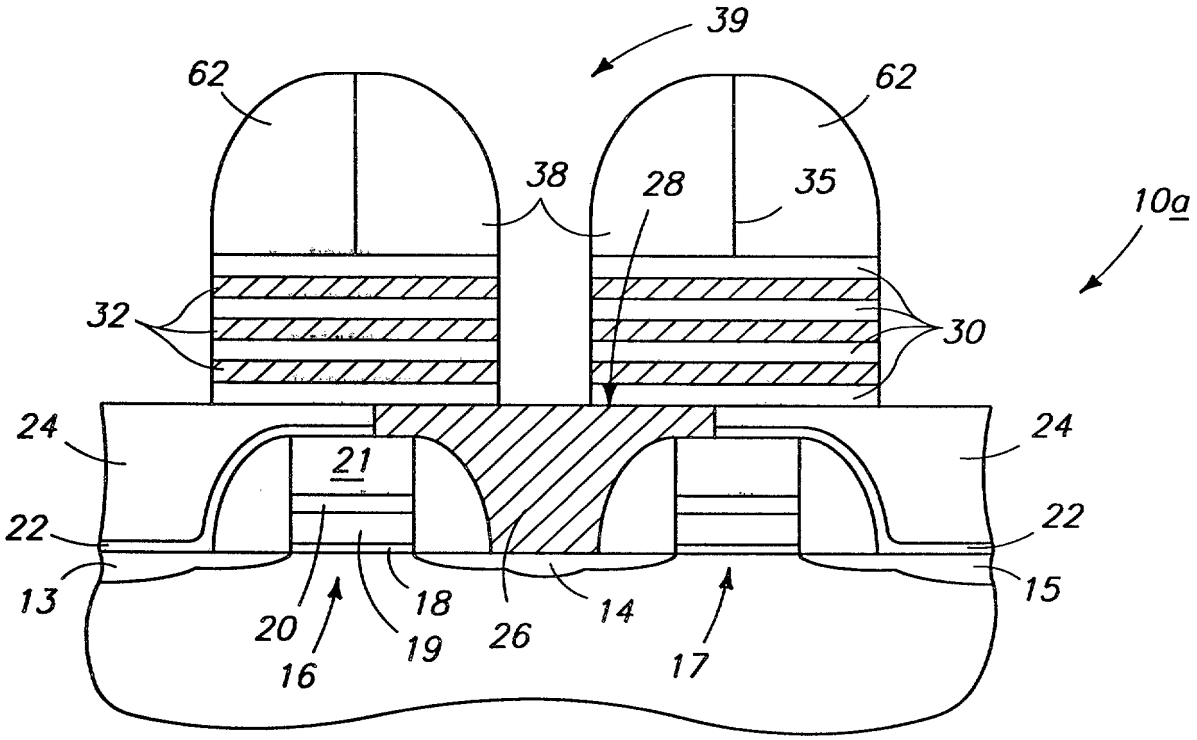

Fig. 15

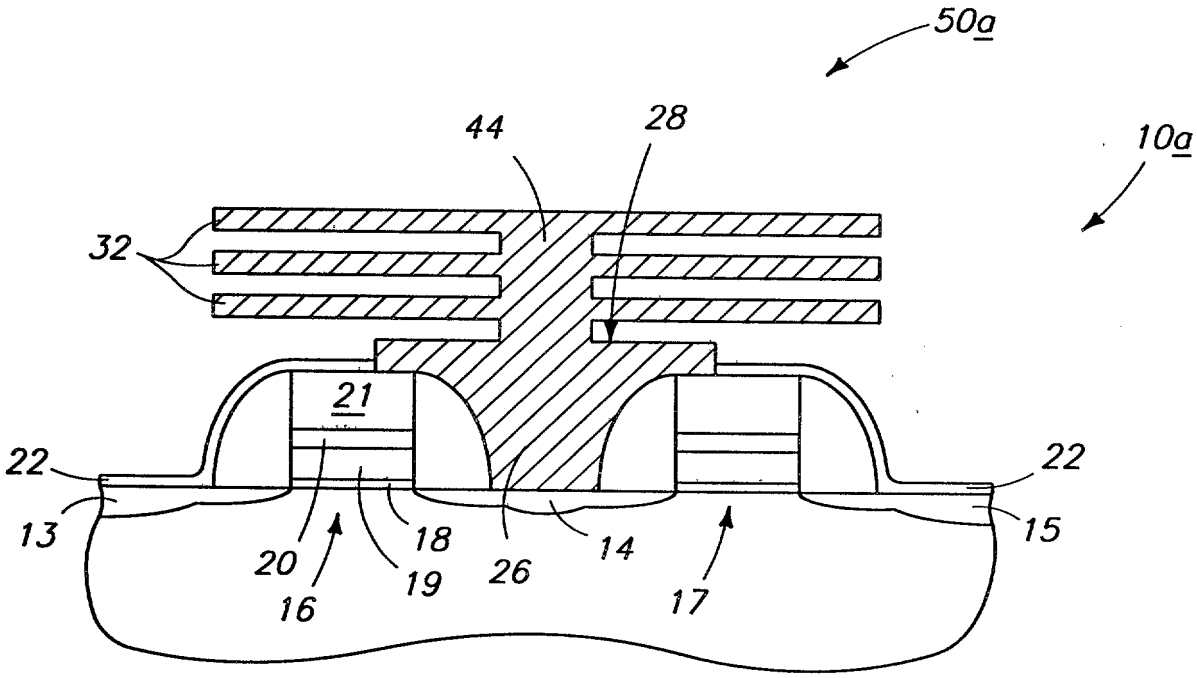

Fig. 1b

AS FILED

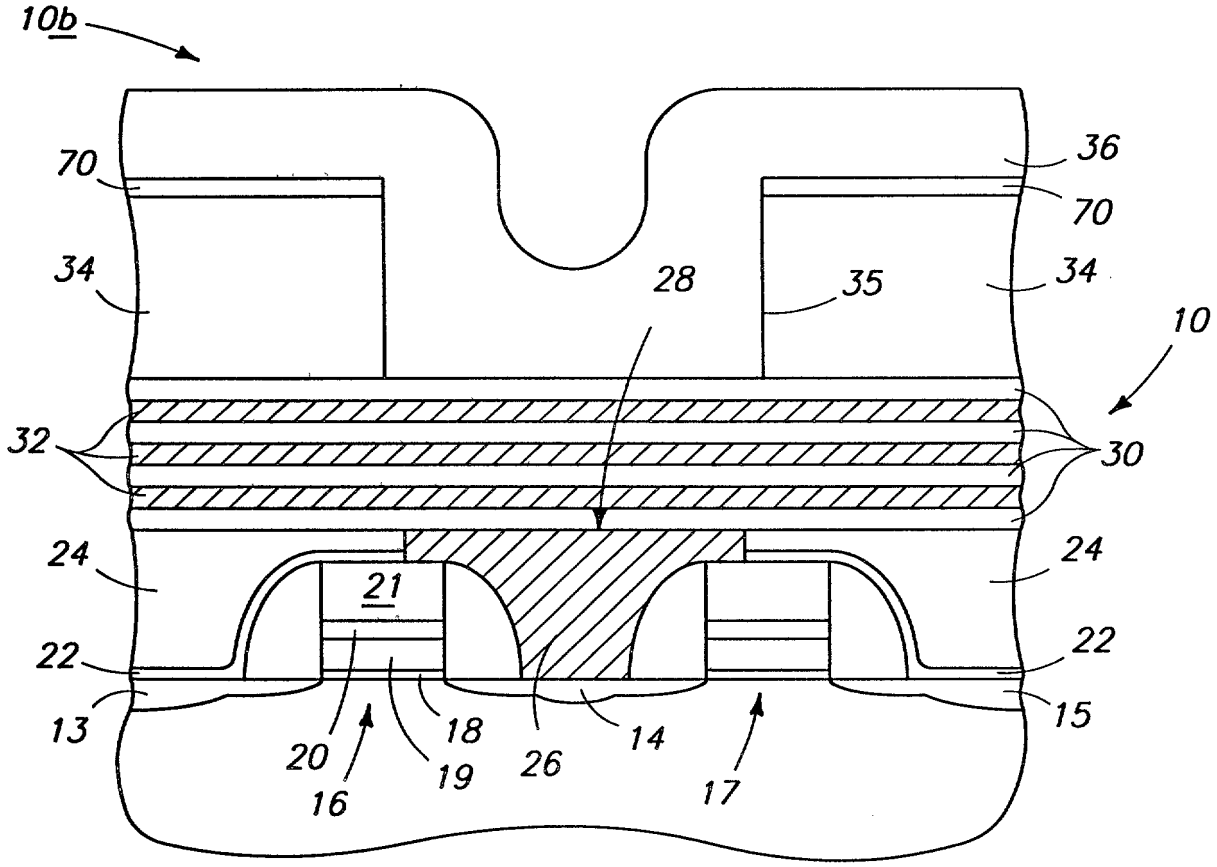

Fig. 11

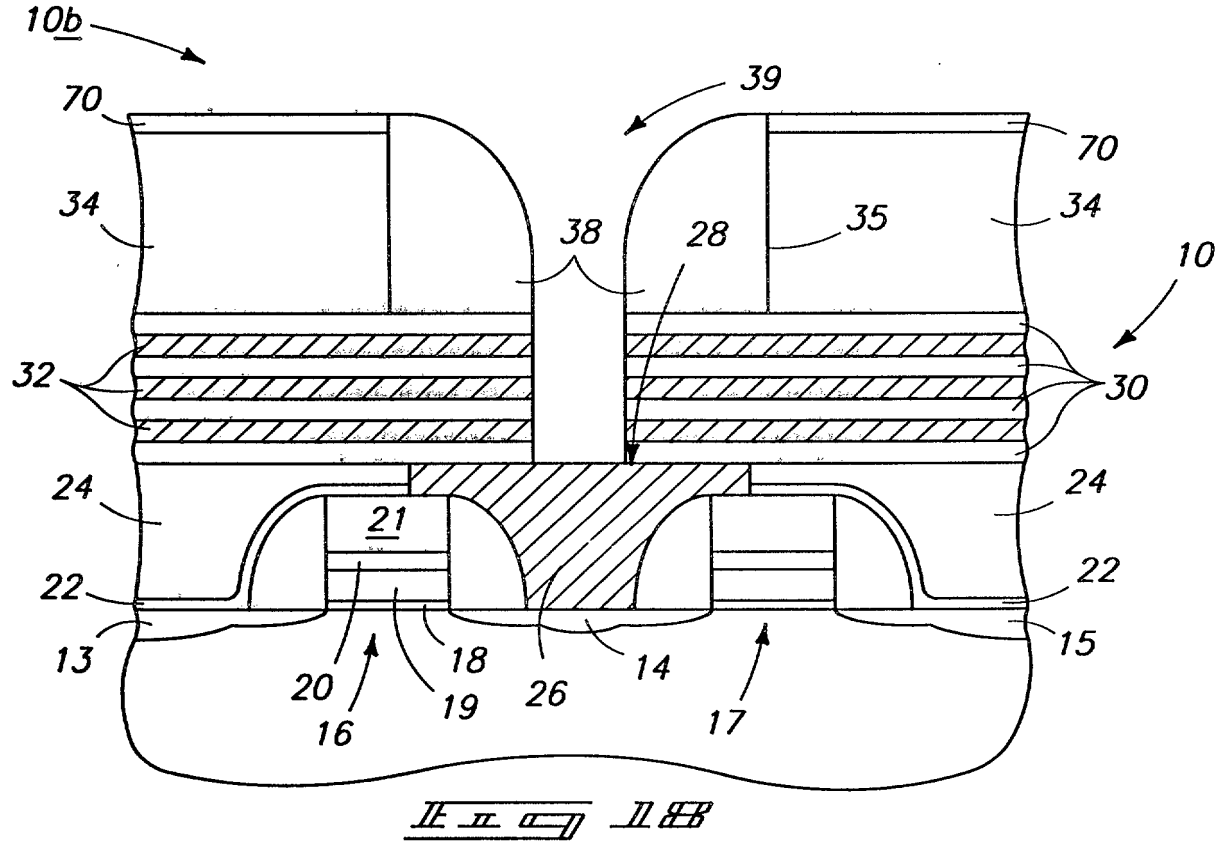

Fig. 11B

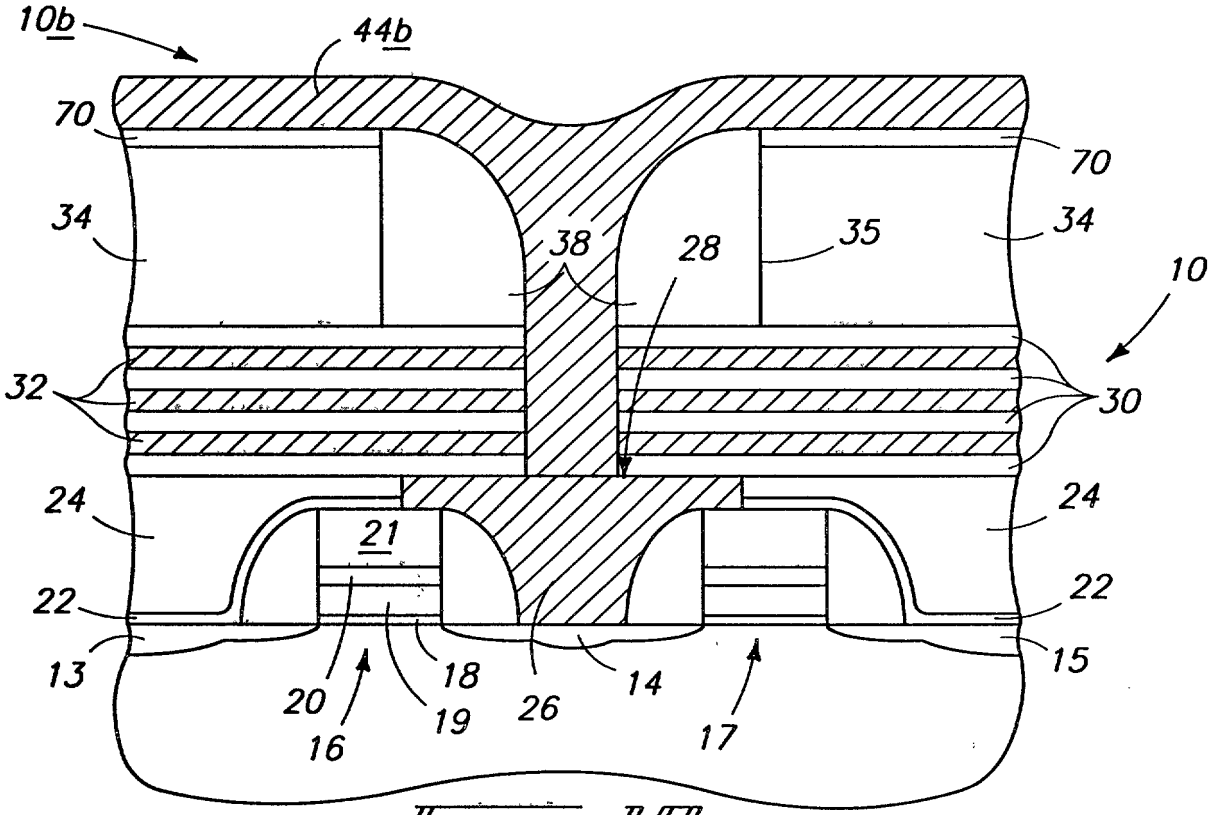

Fig 19

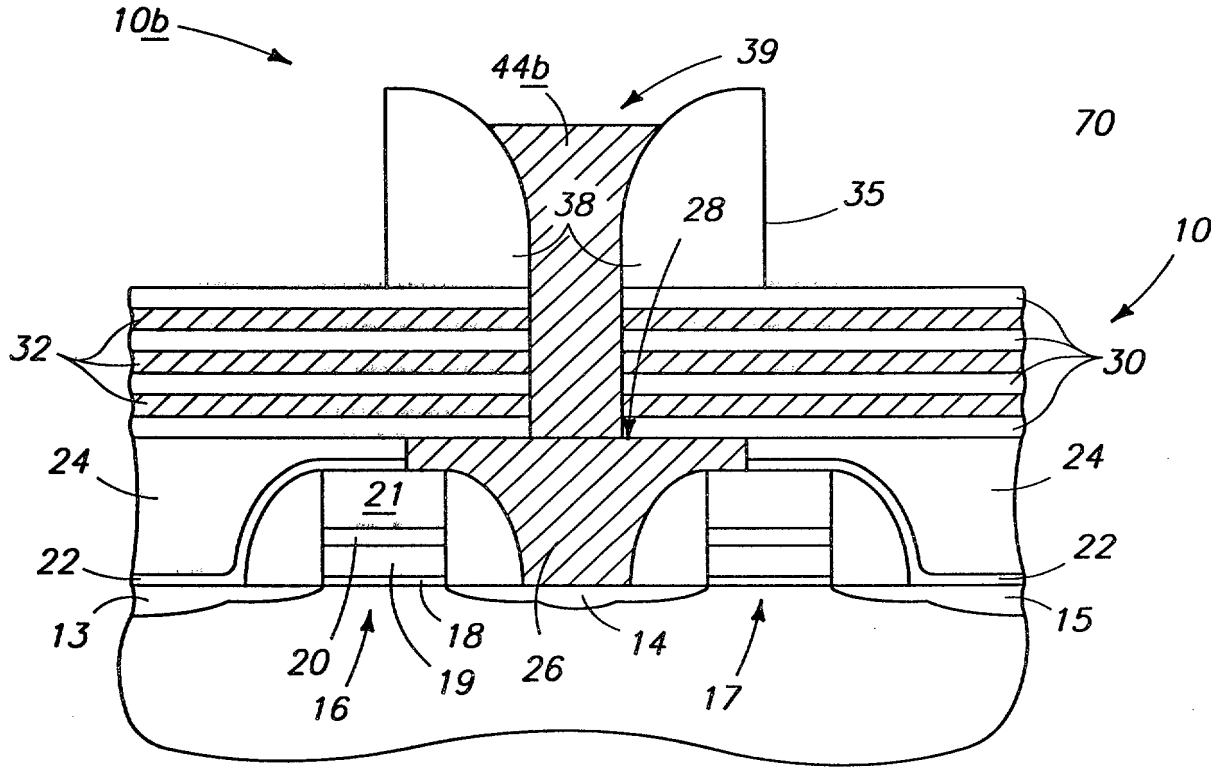

Fig 20

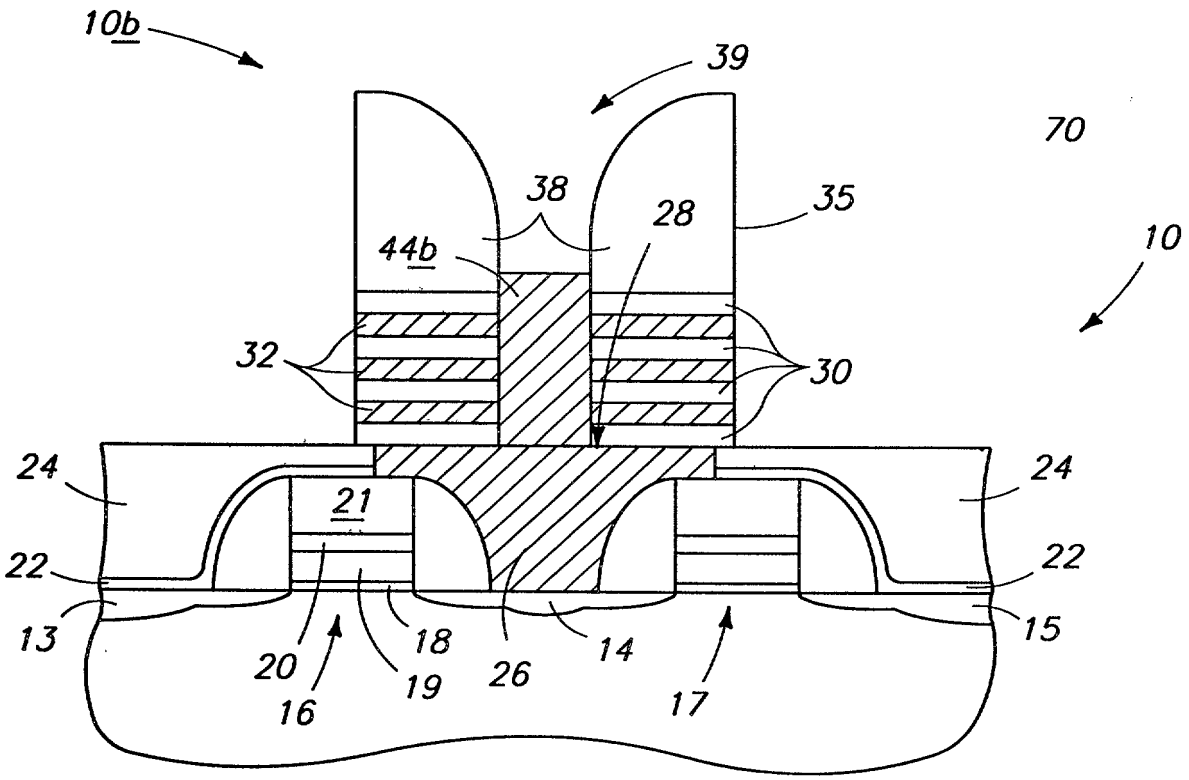
10b
39
70
38
28
35
10
44b
32
30
24
24
21
22
22
13
15
20
16
18
19
26
14
17

Fig 2 II

AS FILED

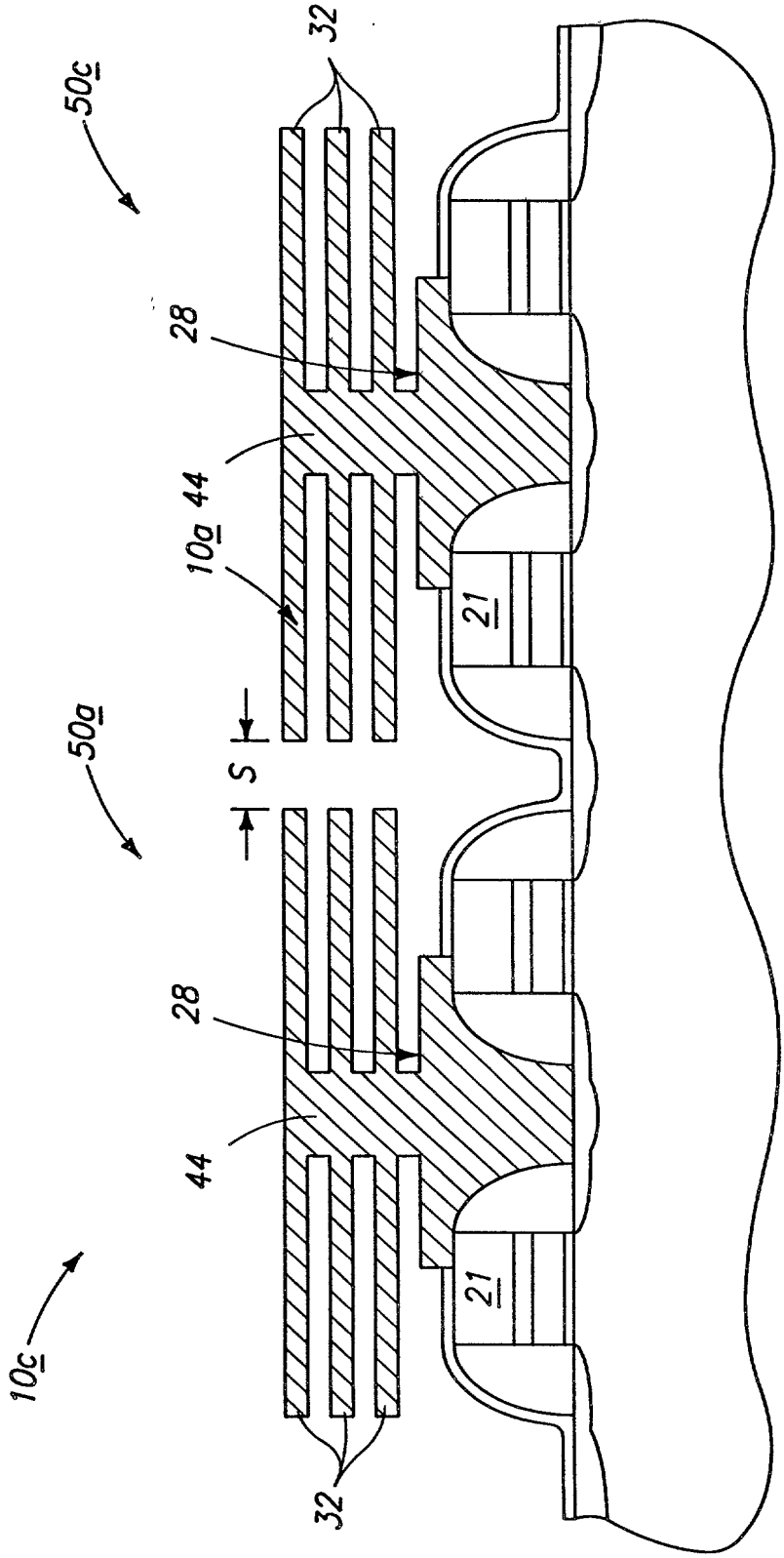

Fig 22